Dr. Emilio Isaac Baungarten Leon

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https://scholar.google.com/citations?user=Hlfj4JgAAAAJ&hl=en

Education

Doctorate in Science in the Specialty of Electrical Engineering, CINVESTAV*, Mexico, 2022 - 2025, thesis: Methodology for implementing SoCs from RTL to GDSII, toward to custom ASICs.
Master of Science in the Specialty of Electrical Engineering, CINVESTAV*, Mexico, 2019 – 2021, thesis: *Acelerador FFT en FPGA Orientado al Procesamiento SAR Aerotransportado.*
* Centro de Investigación y de Estudios Avanzados del Instituto Politécnico Nacional (CINVESTAV)
Biomedical Electronic Engineering, Universidad Autónoma de Guadalajara (UAG), Mexico, 2015 – 2019, thesis: *Metodología para la extracción de modelos tridimensionales basado en estudios de angiografía.*

Work experience

Teacher at Universidad Autónoma de Guadalajara, Department of Diseño Ciencia y Tecnología, 2022 - present.
As a professor at the Universidad Autónoma de Guadalajara, I have delivered courses across multiple engineering disciplines toward digital design area, including Biomedical Electronics Engineering, Software Engineering and Data Mining, Mechatronics Engineering, Industrial and Systems Engineering, and Automotive Technology Engineering.

Intel Corporation — Physical Design Intern**,** *2025 – Present*, Contributing to advanced physical design flows for digital integrated circuits, including floorplanning, placement, routing, and timing closure. Collaborating with senior engineers to validate methodologies and ensure design sign-off readiness within industry-standard EDA environments.

Journal articles

Mascorro-Guardado, Emma, et al. "Edge Detection on a 2D-Mesh NoC with Systolic Arrays: From FPGA Validation to GDSII Proof-of-Concept." Applied Sciences 16.2 (2026): 702. https://doi.org/10.3390/app16020702

Baungarten-Leon, Emilio Isaac, et al. "Comprehensive RTL-to-GDSII Workflow for Custom Embedded FPGA Architectures Using Open-Source Tools." *Electronics* 14.19 (2025): 3866. https://www.mdpi.com/2079-9292/14/19/3866#.

Baungarten-Leon, E. I., Ortega-Cisneros, S., Pinedo-Diaz, G., Rivera-Acosta, M., Rodriguez-Navarrete, F. J., Jaramillo-Toral, U., & Lopez, J. C. G. (2024). Macro Memory Cell Generator for SKY130 PDK. *IEEE Access*, *https://doi.org/10.1109/access.2024.3393479*.

Baungarten-Leon, E. I., Ortega-Cisneros, S., Abdelmoneum, M., Vidana Morales, R. Y., & Pinedo-Diaz, G. (2024). The Genesis of AI by AI Integrated Circuit: Where AI Creates AI. Electronics, 13(9), 1704, https://doi.org/10.3390/electronics13091704.

Mascorro-Guardado, E., Ortega-Cisneros, S., Baungarten-Leon, E. I., Luna-Rodriguez, L. A., Jaramillo-Toral, U., Hernández-Aramburo, M., & Murillo-García, E. (2024). Design and Test of Offset Quadrature Phase-Shift Keying Modulator with GF180MCU Open Source Process Design Kit. Electronics, 13(9), 1705, https://doi.org/10.3390/electronics13091705.

Baungarten-Leon, E. I., Ortega-Cisneros, S., Jaramillo-Toral, U., Rodriguez-Navarrete, F. J., Pizano-Escalante, L., & Panduro, J. R. (2023). Vector Accelerator Unit for Caravel. *IEEE Embedded Systems Letters*, *16*(1), 73-76, https://doi.org/10.1109/LES.2023.3267341.

Baungarten-Leon, E. I., Martín-del-Campo-Becerra, G. D., Ortega-Cisneros, S., Schlemon, M., Rivera, J., & Reigber, A. (2023). Towards on-board sar processing with fpga accelerators and a pcie interface. Electronics, 12(12), 2558, https://doi.org/10.3390/electronics12122558.

Books

Cisneros, S. O., Leon, E. I. B., & Alvarez, P. M. (2025). *INTEGRATED CIRCUIT DESIGN: Tape-out Process with Open-source Tools*. Springer Nature. https://link.springer.com/book/10.1007/978-3-031-92108-7.

Ortega Cisneros, S., Raygoza Panduro, J. J., Baungarten Leon, E. I., & Becerra Alvarez, E. C. (2024). Diseño de Microprocesadores y Aplicaciones de Hardware-Software: Impulsando la Innovación Tecnológica (1st ed.). Centro de Investigación y de Estudios Avanzados del I.P.N. ISBN 978-607-9023-82-9

Patents

Ortega Cisneros, S., Baungarten León, E. I., Rodríguez Navarrete, F. J., González Pérez, M., Pinedo Díaz, G. A., & Rivera Acosta, M. A. (2025). MÉTODO ADAPTATIVO DE CREACIÓN DE COMPILADORES DE MEMORIAS A NIVEL LAYOUT PARA TECNOLOGÍAS MULTIPROPÓSITO UTILIZANDO CELDAS ESTÁNDAR (Patent No. MX/a/2025/00400). Instituto Mexicano de la Propiedad Industrial.

Congress articles

Baungarten-Leon, E. I., & Ortega-Cisneros, S. (2023). "Herramientas de Código Abierto Para el Desarrollo de Circuitos Integrados". XVIII Congreso Concurso de Diseño de Hardware Software Inteligente y Microprocesadores, Diseño de Microprocesadores y Aplicaciones de Hardware-Software: Impulsando la Innovación Tecnológica, pp. 1-5.

Lopez, J. C. G., Ortega-Cisneros, S., Baungarten-Leon, E. I., Vázquez-Robles, M., & Domínguez, J. R. (2024). "Transition from Synchronous to Asynchronous Systems with Minimal Logic Changes". In 2024 IEEE 15th Latin America Symposium on Circuits and Systems (LASCAS), pp. 1-5. IEEE. https://doi.org/10.1109/LASCAS60203.2024.10506182

Baungarten-Leon, E. I., Ortega-Cisneros, S., Torres, C., Jaramillo-Toral, U., Garcia Lopez, J. C., & Raygoza-Panduro, J. J. (2024). "Exploring New Approach With Open Source EDA Tools". Avances En Arquitectura Y Tecnología De Computadores Actas De Las Jornadas SARTECO 2024, pp. 1043-1050. https://doi.org/10.5281/zenodo.13245883

Gonzalez-Perez, M., Ortega-Cisneros, S., Rodriguez-Navarrete, F. J., Pinedo-Diaz, G., Baungarten-Leon, E. I., & Rivera-Acosta, M. (2024, August). RISC-Vcito: A Multicycle Tiny Processor Implemented with SKY130 PDK. In 2024 IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS) (pp. 1388-1392). IEEE. https://doi.org/10.1109/MWSCAS60917.2024.10658692

Jaramillo-Toral, U., Lopez, J. C. G., Ortega-Cisneros, S., Baungarten-Leon, E. I., TorresGonzáles, C., S andoval-Ibarra, F., (2024). "Automated IC Design Flow Using OpenSource Tools and 180 nm PDK", IEEE 67th International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA. https://doi.org/10.1109/MWSCAS60917.2024.10658750

Rivas, D. H. G., Domínguez, J. R., Cisneros, S. O., Zapata, H. E. M., & BaungartenLeon, E. I. (2024, October). "On the Novel Design and FPGA Implementation of a Fuzzy PD Control for a DC Motor". In 2024 21st International Conference on Electrical Engineering, Computing Science and Automatic Control (CCE) (pp. 1-6). IEEE. https://doi.org/10.1109/CCE62852.2024.10770929

Baungarten-Leon, E. I., Ortega-Cisneros, S., Mascorro-Guardado, E., Lopez, J. C. G., Dominguez, J. R., & Panduro, J. J. R. (2025, June). When AI Turns Malicious: Unethical Use of LLMs for Hardware Design. In 2025 23rd IEEE Interregional NEWCAS Conference (NEWCAS) (pp. 606-610). IEEE. https://doi.org/10.1109/NewCAS64648.2025.11107096

Baungarten-Leon, E. I., & Ortega-Cisneros, S. (2025). "Verification and Validation of a CNN IC Created with LLM". XXI Congreso Concurso de Diseño de Hardware-Software Inteligente y Microprocesadores, Auditorio Antonio Alatorre, CUCEI, Universidad de Guadalajara.

U. Jaramillo-Toral, S. Ortega-Cisneros, E. Isaac Baungarten-Leon, and E. JaramilloToral, "Silicluster: A Multi-Module SoC Designed and Fabricated in 180 nm CMOS Using Open-Source Tools for IC Design Democratization," In 2025 IEEE Latin American Electron Devices Conference (LAEDC), Guadalajara, Mexico.

U. Jaramillo-Toral, S. Ortega-Cisneros, E. Isaac Baungarten-Leon, E. Jaramillo-Toral, and H. Emmanuel Muñoz Zapata, "Implementation of a 16:1 Multiplexer and 1:16 Demultiplexer on a Single Chip Using Sky130 PDK and Open-Source EDA Tools for Silicluster," In 2025 IFIP/IEEE 33rd International Conference on Very Large Scale Integration, Puerto Varas, Chile.

J. E. López-Bugarín, L. R. González-Guerra, J. E. Esparza Soto, D. A. García-García, S. Ortega-Cisneros, and E. I. Baungarten-Leon, “An Open-Source Floating-Point Unit IP Core: Design, Verification, and Layout with Sky130,” In 2025 In 2025 IEEE Latin American Electron Devices Conference (LAEDC), Guadalajara, Mexico. https://doi.org/10.1109/LAEDC65721.2025.11289009

U. Jaramillo-Toral, S. Ortega-Cisneros, E. Isaac Baungarten-Leon, E. Jaramillo-Toral & H. Emmanuel Muñoz Zapata, “Analog Blocks for 8-bit SAR ADC: Rail-to-Rail Comparator and Two-Stage Operational Amplifier Designed with Open-Source Tools and Sky130 PDK,” In 21st IEEE Asia Pacific Conference on Circuits and Systems 2025 (APCCAS 2025), Busan, South Korea.

Research Projects

Design of Academic Development Boards, 2025 - 2027
This research project involved the creation, implementation, and validation of two development boards designed for academic use. The first board aimed to provide a cost-effective alternative to commercial FPGAs by featuring a System on a Chip (SoC) with an embedded FPGA and a RISC-V processor, utilizing 130nm technology, and offering sufficient logic capacity for university-level projects. The second board focused on enabling students to deploy neural networks on a portable device, incorporating an AI coprocessor capable of running neural networks using PyTorch libraries, and an SoC with an AI accelerator and a RISC-V processor. Sponsored by SECIHTI in its call for proposals “Ciencia Básica y de Frontera” 2025.

TAE Diseño digital 2025
El proyecto TAE (Talento Altamente Especializado) del COECyTJAL en diseño digital tiene como objetivo fortalecer las capacidades tecnológicas de Jalisco mediante la formación de recursos humanos altamente especializados en el diseño de sistemas digitales y circuitos integrados. El proyecto se centra en el uso de lenguajes de descripción de hardware y metodologías modernas de diseño, con un enfoque práctico orientado a la transferencia de conocimiento, la vinculación con el sector productivo y el impulso a la innovación tecnológica en áreas estratégicas como la electrónica y los semiconductores.

International awards

Método adaptativo de creación de compiladores de memorias a nivel layout para tecnologías multipropósito utilizando celdas estándar (patent no. mx/a/2025/00400). Instituto Mexicano de la Propiedad Industria. Best semiconductor patent 2025.

2023 CSAW AI Hardware Attack Challenge. Sponsored by CSAW & Efabless (2023). Award of $9,750 USD in manufacturing costs. https://www.csaw.io/_files/ugd/acbc49_9d742a8ad9a54e76b29c8e88f111604b.pdf.

2nd AI Generated Design Contest. Sponsored by Efabless (2023). Award of $9,750 USD in manufacturing costs. https://efabless.com/genai/challenges/2-winners.

Professional Skills

Hardware design tools		Software design tools	
Tools:	ISE, Vivado and Vivado HLS	Programing languages:	Assembly, C/C++ (using SIMD instructions), MATLAB and Python
	Quartus and its tool "platform designer"	Architectures	RISC-V and ARM cortex (m0, A9)
HDL:	Verilog, System Verilog (UVM), VHDL and HLS	Programing software	Eclipse, visual studio, and MATLAB
FPGA archt.	Spartan 3-E, 7 Series, Cyclone V, OpenFPGA		
Layout design tools			
OpenLane	RTL to GDSII flow (Synthesis, Design Planning, Placement, CTS, Routing, DRC, LVS)		
OpenROAD GUI	Design Exploration, Timing Closure, DRC, and LVS		
OpenFPGA	Creation of custom FPGA architecture		
Caravel Fusion Compiler	Custom SoC development RTL to GDSII flow (Synthesis, Design Planning, Placement, CTS, Routing, DRC, LVS)		